

01-11-00

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Express Mail Label No. EM401141116US

01/10/00



01/10/00

UTILITY PATENT APPLICATION TRANSMITTAL

Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. DVS-007 (2516/8)
 First Named Inventor Marcel P.J. Gaudreau
 Title High Power Modulator

01/10/00

APPLICATION ELEMENTS

ADDRESS TO: Box Patent Application
 Assistant Commissioner for Patents
 Washington, D.C. 20231

1. ☒ No payment is enclosed at this time.
2. ☒ Specification and Drawings [Total Pages 33]
 Specification - (19 pages)
 Claims - (5 pages)
 Abstract - (1 page)
 Drawings - (8 sheets)
☐ Formal
☒ Informal
3. ☒ Oath or Declaration [Total Pages 4]
 a. ☒ Unexecuted
 b. ☐ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 4 below]

ACCOMPANYING APPLICATION PARTS

7. ☐ 37 CFR 3.73(b) Statement (when there is an assignee)
☐ Power of Attorney
8. ☐ English Translation Document (if applicable)
9. ☒ Information Disclosure Statement (IDS)/PTO-1449
☒ Copies of IDS Citations (AA and CA)
10. ☐ Preliminary Amendment
☐ Drawings [Total Sheets]
☐ Letter to Official Draftsperson Including Drawings [Total Pages]
11. ☒ Return Receipt Postcard

4. ☐ Incorporation by Reference (usable if Box 3b is checked)
 The entire Disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

12. ☒ Unexecuted Small Entity Statement
☐ Statements filed in prior application, (Status still proper and desired)

5. ☐ Microfiche Computer Program (Appendix)

14. ☐ Deletion of Inventor(s)
 Signed statement attached deleting inventor(s) named in the prior application.

6. ☐ Nucleotide and/or Amino Acid Sequence Submission
☐ Computer Readable Copy
☐ Paper Copy (identical to computer copy)
☐ Statement verifying identify of above copies

15. ☒ Patent Application Data Entry Form
 16. ☐ Other:

17. ☐ If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application Serial No. ____/____.
Priority to the above application(s) is claimed under 35 U.S.C. 120.
 Prior application information: Examiner: _____. Group/Art Unit: _____.

18. ☐ Priority - 35 U.S.C. 119
☐ Priority of application Serial No. _____ filed on _____ in _____ is claimed under 35 U.S.C. 119.
☐ The certified copy has been filed in prior U.S. application Serial No. ____/____ on _____.
☐ The certified copy will follow.

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281KR2516/8.915909-1

**STATEMENT CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) & 1.27(c))-- SMALL BUSINESS CONCERN**

Attorney Docket No. DVS-007 (2516/8)

Applicant, Patentee, or Identifier: **Marcel P.J. Gaudreau et al.**
 Application or Patent No.: **Not Yet Assigned**
 Filed or Issued: **January 10, 2000**
 Title: **High Power Modulator**

I hereby state that I am

- ☐ the owner of the small business concern identified below:
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I hereby state that the above identified small business concern qualifies as a small business concern as defined in 37 CFR 1.9(d) and 13 CFR Part 121 for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time, or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby state that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention described in:

- ☒ the specification filed herewith with title as listed above.
☐ the application identified above.
☐ the patent identified above.

If the rights held by the above identified small business concern are not exclusive, each individual, concern, or organization having rights in the invention must file separate statements as to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern, or organization having any rights in the invention is listed below:

- ☐ no such person, concern, or organization exists.
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Separate statements are required from each named person, concern or organization having rights to the invention stating their status as small entities. (37 CFR 1.27).

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b)).

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Correspondence Information

Correspondence Customer Number ::021323

Application Information

Title Line One ::	High Power Modulator
Total Drawing Sheets ::	8
Formal Drawings ::	N
Application Type ::	Utility
Docket Number ::	DVS-007 (2516/8)

Representative Information

Representative Customer Number :: 021323

Field of the Invention

Background

For example, vacuum switch tubes or thyratrons, alone or in combination with Pulse Forming Networks (PFNs) and pulse transformers, have been used to switch high voltage power supplies and high voltage loads, such as gyroklystrons. The non-ideal behavior of tube switches, however, results in numerous undesirable characteristics, such as large effective on-voltage drop, limited current capability and speed, limited Pulse

Repetition Frequency (PRF) capability, high maintenance, and complex driving and protection circuitry. Nevertheless, such switches have provided a nearly exclusive solution to the problem of high-voltage switching until recently.

Typical tube switches use a single device to switch the entire switching voltage.

5 Consequently, the high voltage capability of most tube switches is limited to the high voltage capability of a single tube. This limits the reliability and flexibility of high voltage systems using these tubes. Thus, as new system requirements extend to higher voltage or power, the use of tubes becomes increasingly problematic.

Summary of the Invention

10 The present invention relates to a high power modulator that uses semiconductor devices as a cost-effective alternative to high voltage tubes. Using solid state semiconductor devices results in a simpler modulator design with higher reliability, higher efficiency, and lower cost. Solid state devices are generally low voltage devices. However, recent advances in semiconductor device technology have resulted in devices
15 such as the Insulated Gate Bipolar Transistor (IGBT) which have improved voltage and current handling characteristics. Presently typical commercial IGBT devices can each be used to switch voltage from 600V to 6000V.

IGBTs have the high current handling capability of bipolar transistors (50-1200A), combined with the very low drive current requirements of field effect
20 transistors (FETs). These devices eliminate the need to have cascaded stages of bipolar

drives within the device itself, which were required because of the low betas of prior art high-current bipolar circuit designs.

IGBTs can be used for high voltage switching by connecting many devices in series. This technique is described in, for example, U.S. Patent No. 5,444,610 (hereinafter “the ‘610 patent”), which is assigned to the assignee of the present application, and which is incorporated herein by reference. The ‘610 patent describes a high power modulator capable of switching high voltages using large numbers of low voltage switches connected in series, where each of the switches is connected in parallel with a voltage limiting means. This technique provides the flexibility of a modular design with no inherent limit to voltage handling, because the voltage limiting means described in this patent has virtually unlimited voltage and current carrying capability.

For some applications, however, the apparatus described in the ‘610 patent may be physically large and expensive to manufacture. For example, to switch 120 kV, up to 160 series connected IGBTs may be required, which presents size and configuration challenges. In addition, so that no single IGBT sees harmful or destructive voltages, the load must be shared equally among each IGBT device. Therefore, the gate drives for the IGBT devices must be highly synchronized.

Thus, an object of the present invention is to incorporate serially connected low voltage switches having load sharing features in a compact, transformer coupled gate switch. By floating each IGBT and its respective gate drive circuitry with respect to ground, and by ensuring that all power and control connections to the IGBT and its gate

drive are isolated, no single IGBT will experience a voltage greater than its design limit.

In addition, the IGBT devices can be highly synchronized and, therefore, can switch substantially simultaneously.

Thus, the present invention features a modulator that comprises one or more
5 transformers and a plurality of switches. The transformers comprise a primary and a plurality of secondary windings. Each secondary winding has an output terminal pair. Each of the plurality of switches is associated with a respective secondary winding and has input and output terminals and a control terminal. The control terminal of each switch is in electrical communication with a respective output terminal of the plurality of
10 secondary windings. When an input signal is applied to the primary of the transformer, a signal is induced in the secondary such that the plurality of switches, which are each coupled to a respective secondary winding, are switched substantially simultaneously.

In one embodiment, the modulator further comprises a stack of modulators sharing the same primary. In other embodiments, the modulator further comprises at
15 least one voltage limiter, such as a Zener diode or snubbing circuit, and in one embodiment the at least one voltage limiter is connected in parallel with at least one of the plurality of switches. In another embodiment, the plurality of switches are connected in series or in parallel according to the configuration of the load. In further embodiments, at least one of the plurality of switches comprises a transistor, such as an insulated gate
20 bipolar transistor (IGBT), an avalanche-rated field effect transistor (FET), or a power metal oxide FET (MOSFET).

The present invention also features a modulator comprising a transformer, a plurality of retriggerable drive circuits, and a plurality of switches. The transformer includes a primary and a plurality of secondary windings. Each of the plurality of retriggerable drive circuits has an output and is electrically connected to a respective one of the plurality of secondary windings. Each of the plurality of switches is associated with a respective retriggerable drive circuit and has two output terminals and a control terminal. The control terminal of each switch is in electrical communication with a respective output terminal of the retriggerable drive circuit with which it is associated. In one embodiment of the invention, the modulator comprises a stack of modulators sharing the primary of the transformer. In operation, when an input signal is applied to the primary of the transformer, each of the plurality of switches is switched substantially simultaneously and remains substantially on until a second signal is applied to the primary of the transformer to turn the switches off.

The present invention also features a method of switching a signal. An input signal is applied to the primary of a transformer. In response to this input signal, a voltage is induced in a plurality of secondary windings of the transformer. This induced voltage switches, substantially simultaneously, each of a plurality of switches that are electrically controlled by a respective one of the plurality of secondary windings. In one embodiment of the invention, each of the plurality of switches is maintained in a substantially conducting state after termination of the input signal. In another embodiment, a reset input signal is applied to the single primary winding of the transformer.

The present invention also features a modulator that may be used as a very large, very fast series switch, or circuit breaker that enables high power systems to turned on and off in a rapid, repeatable, and controllable way. When the modulator is used as a switch, power can be substantially removed from the load when the switch is 'off' or
5 open.

The foregoing and other objects, aspects, features, and advantages of the invention will become more apparent from the following description and from the claims, when viewed in conjunction with the accompanying drawings.

Brief Description of the Drawings

10 Fig. 1 is a simplified schematic diagram of a modulator with switches connected in series, in accordance with one embodiment of the invention.

Fig. 2 is a simplified schematic diagram of a modulator with switches connected in series that includes voltage limiting means, in accordance with the invention.

Fig. 3 is a simplified schematic of one embodiment of a modulator with series
15 connected switches, in accordance with the invention.

Fig. 4 is a simplified schematic diagram of a modulator having switches connected in parallel, in accordance with an embodiment of the invention.

Fig. 5 is a three dimensional diagram of one embodiment of the modulator of the present invention.

Fig. 6 is a simplified schematic of a modulator that includes stacked modulators, in accordance with the invention.

Fig. 7 is a simplified schematic of a retriggerable modulator, in accordance with an embodiment of the invention.

5 Fig. 8 is a simplified schematic of another implementation of a retriggerable modulator, in accordance with an embodiment of the invention.

Detailed Description

Modulators are electronic devices used to precisely regulate the delivery of high voltage, high current electrical pulses. A modulator can act as a simple switch between a
10 high power supply and its load (such as a klystron). Ideally, modulators have infinite voltage holdoff, infinite off-resistance, zero on-resistance, and full immunity to transients and voltage reversals. Modulators are critical components of electronic systems used for numerous applications such as radar systems, particle accelerators, medical diagnostics and treatment equipment, and manufacturing equipment, such as ion implantation for
15 semiconductor fabrication. In addition, new processes for food sterilization, waste treatment, and pollution control are also being developed which require the use of high power modulators.

Many high power modulators use pulse transformers to allow switching of the required pulse energy at low voltage. However, conventional pulse modulators generally
20 require large subsystems and vacuum tubes, alone or in combination with pulse-forming

networks (PFN's) to drive the pulse transformer. A pulse forming network (PFN) modulator is an electronic device used to precisely regulate the delivery of high voltage, high current electrical pulses.

Achieving a nearly ideal pulse is critical to the performance of a number of pulsed power applications. An "ideal pulse" has instantaneous rise and fall time and a flat top, independent of load current and repetition rate. In ion implantation applications, for example, it is critical to minimize the voltage drop and pulse-to-pulse voltage variation to achieve uniform processing. This requires very fast rise and fall times to minimize the energy provided at voltages other than the amplitude of the pulse. It also requires a very flat-top for the pulse, with no ripple or droop. In radar applications, the rise and fall times must be within the amplifiers' operating parameters. The flat top is very critical to parameters such as phase noise. Generating pulses that most closely approach the ideal pulse waveform is, therefore, often a critical objective of high pulsed power system design.

Historically, vacuum switch tubes or thyratrons, alone, or in combination with PFNs and pulse transformers, have been used to generate pulse waveforms. These conventional switches have non-ideal behavior, such as a large effective voltage drop, limited current capability and speed, high maintenance, and complex driving and protection circuitry. Nevertheless, they have provided a nearly exclusive solution to the problem of high-voltage switching until recently because no cost effective alternatives were available. As future system requirements extend to higher voltage and power,

however, the use of switch tubes becomes increasingly impractical due to the inherent voltage and current limits of these devices.

The physical size of prior art power modulator systems, moreover, generally is very large, which is problematic for many applications. Furthermore, the expected lifetime of conventional power modulator systems using vacuum tubes and pulse forming networks is generally low. To meet these and other needs, the present invention, provides a reliable, fast, compact, low-current, transformer coupled gate switch technology modulator.

The present invention features a solid state modulator that can be used in systems that would otherwise require a switch tube, spark gap, or thyatron pulse forming network (PFN) modulator to switch high voltage and power. Fig. 1 illustrates a modulator according to the present invention that is connected between a power source 21 and a load 14. The modulator 10 includes a transformer 16 connected to the trigger source 12, and a plurality of switches 18 connected in series. The transformer 16 further includes a primary winding 20 and a plurality of secondary windings 22. The primary winding 20 may be connected to ground potential while the plurality of secondary windings 22 may float at staggered high voltages. In one embodiment of the invention, the primary winding 20 further includes an input terminal and each secondary winding 22 further includes an output terminal.

In addition, although the primary winding 20 is illustrated in Fig. 1 as a single winding, in other embodiments of the invention, the primary winding 20 is a plurality of

windings that achieve a predetermined turns ratio (i.e. 2:1 or 4:1). In another embodiment, the primary winding 20 may be a portion of a winding such as a half-turn of a winding. In another embodiment the primary winding 20 is a distributed primary winding. Distributing the winding can improve geometrical packing and reduce leakage inductance.

The transformer 16 can be formed using a toroidal core comprising a high permeability material such as ferrite. Using a toroid provides the advantage that the length of wire forming each secondary winding 22 will be the same, so that the switches 18 will turn off and on at the same time. In another embodiment (as described in connection with Fig. 6), the modulator 10 includes one or more modulators stacked together, with the transformer 16 of each modulator sharing the same primary winding 20. In one embodiment, the stacked modulator configuration comprises stacks of toroids forming the transformers 16 of the modulators. Stacking the toroids is advantageous because it helps to reduce leakage inductance.

Each switch 18 is associated with a respective secondary winding 22. In one embodiment (not shown), each switch is electrically coupled to a respective output terminal of the respective secondary winding 22. Each switch 18 includes a transistor, such as an insulated gate bipolar transistor (IGBT), an avalanche FET, or a power MOSFET. For example, a modulator 10 may include an arbitrary number of switches 18, such as IGBTs, connected in parallel and/or in series (which is explained further below). In one embodiment, the switches 18 include a combination of different types of switches,

such as a combination of IGBTs and avalanche FETs. In one embodiment, each switch 18 includes a voltage limiting means.

Power MOSFETs, unlike conventional bipolar transistors, are essentially voltage driven devices. Moreover, because power MOSFETs are majority carrier devices and have minimal minority carrier storage time, power MOSFETs have exceptionally fast rise/fall times. Power MOSFETs also are rugged switching devices because they lack the secondary breakdown effect of bipolar transistors.

In comparison, IGBTs have the high input impedance and high speed characteristics of a MOSFET with the conductivity characteristics of a bipolar transistor. In addition, IGBTs can be turned on and turned off electronically, in contrast to thyristor switches conventionally used in some power modulators, which can only be turned on electronically. The fact that IGBT and MOSFET switches turn off electronically with low-power pulses eliminates the need for PFNs in the modulator.

IGBT switches may be characterized by a low voltage drop, for example about 2.5 Volts, so that in saturation the IGBT is essentially a Darlington pair configuration with a FET as the input stage and a bipolar power transistor for the output stage. The risetime of IGBTs is largely determined by the gate drive circuitry, as described below.

In another embodiment, each switch 18 includes avalanche FETs, such as a thousand volt FET with an avalanche rating. A typical avalanche FET could have a saturated on-state resistance of 2Ω and a switching time of about 30 nsec, both of which are sufficient for the modulator applications described herein.

When the switches 18 are connected in series, as illustrated in Fig. 1, each individual series connected switch 18 operates with a floating ground reference. Consequently, all switches will perform identically and none should experience any voltage greater than its design limits regardless of the end of the series stack at which it is located. Each switch 18 and its gate drive circuitry (not shown) can “float” relative to ground, and all power and control connections to the switches 18 may be made inductively. Thus, in the embodiment illustrated in Fig. 1, a trigger can be applied at the input 12 and power 21 can be applied to the switch 18. In response to the power applied and a trigger at the primary, a voltage is induced at each secondary 22 of the transformer at substantially the same time. Thus, each switch 18 will be switched substantially simultaneously.

In one embodiment, the switch 18 is an IGBT, the FET inputs (i.e., the gate signals) are electrically coupled in parallel to the transformer 16 and the outputs of each switch 18 are connected in series or in parallel with the load 14. The primary winding 16 of the transformer is at ground potential and the secondary windings 22 are floating at staggered high voltages. For a typical IGBT switch, the gate capacitance for each IGBT is approximately 5 nF. During operation, the entire modulator 10 acts as a high voltage switch, so that when an input signal is applied at trigger 12 and power 21 is applied to the switches 18 are switched substantially simultaneously. Because the switches are in series, very high voltages can be switched. For example, if switch 18 is a 1200V IGBT switch and three windings are used as shown in Fig. 1, the circuit of Fig. 1 can switch

3600V by switching 1200 V across each switch 18. Additional switches can be added to switch even higher voltages.

In some embodiments of the invention, the modulator 10 can further include one or more voltage limiting devices to protect the switches 18. Fig. 2 illustrates a modulator 10 that includes a plurality of voltage limiting devices 24. Each voltage limiting device 24 is connected in parallel with a respective switch 18.

The voltage limiting device 24 is preferably integrated into the switch 18 itself. Numerous other voltage limiting devices can also be used, such as a Zener diode, a snubbing circuit (such as described in the '610 patent), and a clamping circuit. For example, the voltage limiting means can be a metal-oxide varistor (MOV) or a capacitor connected in parallel with a series combination of a dissipating resistor and a switch (such as described in the '610 patent).

In another embodiment, the switch 18 comprises an avalanche-rated FET that has a voltage limiting capability. Regardless of the type of voltage limiting technique used, if the voltage applied to the switch 18 is above a predetermined value, then the current induced by the input 12 will be conducted through the voltage limiting device 24. The corresponding voltage drop across the voltage limiting device 24, however, will be independent of the current conducted therethrough

Fig. 3 illustrates a schematic diagram of one embodiment of the modulator 10, in accordance with the present invention. Eleven IGBT switches 28 are shown to be connected in series and are driven by parallel 1:1 windings. It should be understood,

however, that the illustrations of this figure, including the windings on the transformer, are provided by way of example only. Numerous other configurations of windings can be used. For example, better geometrical packing of the windings can reduce transformer leakage. This can be accomplished by using a distributed primary winding, or by using
5 additional windings (i.e. 2:1 or 4:1).

In addition, because leakage inductance impacts the induced current (and, consequently, the voltage) achievable into the primary, the turns ratio can be adjusted for step-down operation with higher voltage primary drive. For example, a 4:2 step down can be used with a 35 Volt drive on the transformer. In another example, the transformer
10 16 can be made from a ferrite toroid, and the ferrite toroid can be biased at the midpoint of the switches 18.

In another embodiment (not shown), the transformer 16 can have multiple primary windings in parallel to improve geometrical packing (and reduce leakage inductance), and through the use of much higher voltage gate drive circuitry. This technique helps to
15 offset the voltage current induction limitations of the leakage inductance without adding capacitance to the circuit.

The series connection of switches illustrated in Figs. 1, 2, and 3 provide increased voltage handling capability. Fig. 4 illustrates another embodiment of the invention wherein the switches 18 are connected in parallel, to provide increased current handling
20 capability. In this embodiment, a control signal, such as a trigger, is applied at input 12, and this signal is coupled substantially simultaneously to each switch 18, so that the

switches 18 can substantially simultaneously switch current from the power source (current source) 21'. The ability to substantially simultaneously switch current from the power source increases the current handling capability of the modulator 10.

Fig. 5 is a three dimensional diagram of one embodiment of the modulator of the present invention. The modulator 50 includes a transformer 16 formed of a ferrite toroid core 17. As described above, using a toroid core is advantageous because the length of wire forming each secondary winding 22 can be substantially the same. This will enable each switch 18 to turn off and on at substantially the same time. Switches 18 are positioned around the toroid core 17 and are connected to the secondary windings 22 as described above.

The modulator 50 can be surrounded by an epoxy casting 54, as illustrated in Fig. 5. Power and load terminals 56 may be positioned at the edges of the epoxy casting 54. The modulator 50 of Fig. 5 is particularly suitable for stacking multiple modulators as described below in connection with Fig. 6.

Fig. 6 is a simplified schematic of a modulator 10 that includes stacked modulators that share the same primary winding 20 in accordance with the invention. Each switch 18 may include voltage limiting means (not shown). The ability to stack modulators and use the same primary winding to substantially simultaneously switch all switches in each of the modulators is particularly advantageous. By stacking modulators, one skilled in the art can scale the modulator power level to desired levels of power and/or voltage without the limitations of the prior art.

Thus, in the configurations described above, the present invention provides a very fast high-voltage switch. There are several advantages of modulators of the present invention. For example, the modulators of the present invention can replace 'crowbars' in vacuum tube applications, because they can typically open and close in less than 0.5 μ S. If either instantaneous or average current through the switch rises above pre-set limits, the modulator simply opens, removing power from the load. The delay from sensing of an over-current condition, such as an arc, to the opening of the switch, can be kept well below 1 μ S. Another advantage is that the 'opening' of the solid state switch does not shut down power supply operation, as with most conventional crowbars. The modulators of the present invention may also be used as circuit breakers. Because these switches are both opening and closing switches, power can be substantially removed from the load when the switch is 'off', or open.

When the modulator of the present invention is used as a pulse modulator, the opening and closing of the modulator is controlled by a command signal at low voltage that is applied to the primary of the transformer. The result is a stream of high power pulses into the load, each with rapid rise and fall times, and extremely consistent pulse-to-pulse characteristics.

As described previously, consistent pulse-to-pulse characteristics and fast rise times are very desirable for many applications. Thus, because the switch design and construction is identical in both a pulsed application and as a series switch, the modulator of the present invention can be used simultaneously as a pulse modulator and as a fast fault protection disconnect system. This can significantly simplify the overall design of

systems that incorporate such modulators. Because solid state modulators do not use resonant circuits, each pulse can be arbitrarily sized. This allows complete pulse width and separation flexibility from 30nS to DC.

Accordingly, in another aspect, the invention features a modulator capable of switching power to meet rigorous pulse width agility requirements. In this aspect of the invention, the modulator is retriggerable. Fig. 7 is a simplified schematic of a retriggerable modulator 10, in accordance with an embodiment of the invention. This modulator includes a transformer 16, a plurality of retriggerable drive circuits 28, and a plurality of switches 18.

The transformer 16 is configured as described previously in connection with Figs. 1 through 4. Each retriggerable drive circuit 28 is electrically connected with a respective one of the plurality of secondary windings. Each switch 18 has input and output terminals and a control terminal and is associated with a respective retriggerable drive circuit 18. The control terminal of each switch 18 is electrically connected with the output of the respective retriggerable drive circuit 28.

During operation, when a first control signal is applied to the primary of transformer 16 via the input 12, a voltage is induced in each secondary of the transformer 16. Then, each of the plurality of switches 18 is substantially simultaneously switched by the first signal applied to the primary and remains substantially on until a second signal is applied to the primary of the transformer 16. During this time, each switch 18 can switch the power from power supply 21.

Once a switch 18 is switched on, it is not necessary to hold it in the “on” position once switching is complete. Because the input of the switch looks like a capacitor to the secondary of the transformer 18, large drive currents are only necessary to charge this capacitance quickly, but no drive current is necessary to sustain it. Thus, in theory, the gate pulse can be turned off, and the switch 18 will remain on until a negative pulse is provided. In practice, however, the transformer flux will reset, pulling the gate on the control input of the switch 18 negative by a small amount and shutting down the switch 18. In addition, the gate capacitance of the switch 18 is accompanied by a finite leakage, which will eventually increase the “on” state conduction losses and finally shut down the pulse. Both of these problems can be overcome by using the retriggerable drive circuit 28 of Fig. 7.

In operation, a gate pulse, such as a positive going pulse, passes transparently through the series FET and Zener diode of each of the retriggerable drive circuits 28, so each of the switches 18 will be switched on substantially simultaneously. When the gate pulse ends, or the core of transformer 16 saturates. However, the reset voltage is insufficient to conduct through the series Zener (which has a blocking voltage of about 5V) of the retriggerable drive circuit 28. Therefore, the series FET of the retriggerable drive circuit 28 blocks the reverse bias during reset. In this manner, each switch 18 remains on either until a negative-going “end of pulse” trigger is sent through the primary, or until the gate charge leaks away.

Fig. 8 illustrates an alternate embodiment of the retriggerable switch. The retriggerable switch of Fig. 8 includes a bipolar voltage limiting means electrically

connected in series with a gate circuit, such as back-to-back Zener diodes. In this circuit, the series FET is not required, and the gate is kept at negative voltage in the off-state for better noise immunity. This circuit requires a larger drive voltage, which also improves noise immunity.

- 5 In another embodiment, a control circuit (not shown) can be used to generate “retrigger” pulses at specified intervals, thus recharging the control input of each switch 18 and extending the high voltage pulse as long as desired.

- While the preferred embodiments have been shown and described, it should be understood that there is no intent to limit the invention by such disclosure, but, rather, is
10 intended to cover all modifications and alternate constructions falling within the spirit and scope of this invention.

What is claimed is:

1. A modulator comprising:

a) a transformer comprising a primary and a plurality of secondary windings, each secondary winding having an output terminal; and

5 b) a plurality of switches, each switch associated with a respective secondary winding and having input and output terminals and a control terminal, the control terminal of each switch being in electrical communication with a respective output terminal of the plurality of secondary windings,
wherein the plurality of switches are substantially simultaneously switched by
10 an input signal applied to the primary.

2. The modulator of claim 1 wherein the transformer further comprises a toroidal core.

3. The modulator of claim 1 wherein a length of wire forming each of the plurality of secondary windings is substantially the same, wherein each of the plurality of switches turns off and on at substantially the same time.

15 4. The modulator of claim 1 wherein the transformer further comprises a ferrite core.

5. The modulator of claim 1 further comprising at least one voltage limiter in parallel with at least one of the switches.

6. The modulator of claim 5 wherein the voltage limiter comprises a Zener device.

7. The modulator of claim 5 wherein the voltage limiter further comprises a snubbing
20 circuit.

8. The modulator of claim 5 wherein the voltage limiter comprises a metal oxide varistor.

9. The modulator of claim 5 wherein the at least one voltage limiter is connected across the input and output terminals of at least one of the plurality of switches.
10. The modulator of claim 1 wherein the plurality of switches are connected in parallel.
11. The modulator of claim 1 wherein the plurality of switches are connected in series.
- 5 12. The modulator of claim 1 wherein the plurality of switches are connected in a series/parallel combination.
13. The modulator of claim 1 wherein at least one of the plurality of switches comprises an avalanche-rated field effect transistor.
- 10 14. The modulator of claim 1 wherein at least one of the plurality of switches comprises an insulated gate bipolar transistor.
- 15 15. The modulator of claim 1 further comprising a logic gate circuit in electrical communication with an input terminal of the primary winding.
16. The modulator of claim 1 wherein the primary winding further comprises an output terminal at ground potential.
- 15 17. The modulator of claim 1 wherein the primary winding comprises a distributed primary winding.
18. The modulator of claim 1 wherein the primary winding comprises a plurality of windings connected in parallel.
19. A modulator comprising:
 - 20 a) a transformer comprising a primary and a plurality of secondary windings, each secondary winding having an output terminal;

b) a plurality of retriggerable drive circuits, each of the retriggerable drive circuits being electrically connected with a respective one of the plurality of secondary windings and having an output; and

c) a plurality of switches, each switch associated with a respective retriggerable drive circuit and having two output terminals and a control terminal, the control terminal of each switch being in electrical communication with a respective output terminal of the retriggerable drive circuit,

wherein each of the plurality of switches is substantially simultaneously switched by a first signal applied to the primary and remains substantially on until a second signal is applied to the primary of the transformer.

20. The modulator of claim 19 wherein at least one of the first and second signals comprises a negative going signal.

21. The modulator of claim 19, wherein at least one of the first and second signals comprises a positive going signal.

22. The modulator of claim 19 wherein at least one of the first and second signals comprises a pulse.

23. The modulator of claim 19 wherein the first signal is different than the second signal.

24. The modulator of claim 19 wherein the transformer further comprises a toroidal core.

25. The modulator of claim 19 wherein the modulator comprises a stack of modulators sharing the primary of the transformer.

26. The modulator of claim 19 wherein each secondary winding of the transformer controls a respective plurality of switches.

27. The modulator of claim 19 wherein at least one of the plurality of switches comprises an avalanche-rated field effect transistor.
28. The modulator of claim 19 wherein at least one of the plurality of switches comprises an insulated gate bipolar transistor.
- 5 29. The modulator of claim 19 wherein at least one of the plurality of retriggerable drive circuits comprises a Zener diode connected in series with a field effect transistor.
30. The modulator of claim 19 wherein at least one of the plurality of retriggerable drive circuits comprises a bipolar voltage limiting means.
31. A method of switching a signal, the method comprising the steps of:
- 10 a) applying an input signal to a primary of a transformer;
- b) inducing a voltage in a plurality of secondary windings of the transformer in response to the input signal; and
- c) switching, substantially simultaneously, each of a plurality of switches that are electrically controlled by a respective one of the plurality of secondary
- 15 windings of the transformer, in response to the single input signal.
32. The method of claim 31, further comprising the step of maintaining each of the plurality of switches in a substantially conducting state after termination of the input signal.
33. The method of claim 31, further comprising the step of applying a reset input signal
- 20 to the single primary winding of the transformer.
34. A modulator comprising:
- a) a plurality of stacked transformers sharing the same primary, wherein the primary comprises at least one winding and each transformer further comprises

a plurality of secondary windings, each secondary winding having an output terminal;

- 5 b) a plurality of switches, each switch associated with a respective secondary winding and having input and output terminals and a control terminal, the control terminal of each switch being in electrical communication with a respective output terminal of the plurality of secondary windings,

wherein the plurality of switches are substantially simultaneously switched by an input signal applied to the primary.

ABSTRACT

A compact transformer coupled modulator is described. The modulator includes a transformer comprising a primary and a plurality of secondary windings, where each secondary winding has an output terminal. The modulator also includes a plurality of switches, where each switch is associated with a respective secondary winding and has input and output terminals and a control terminal. The control terminal of each switch is in electrical communication with a respective output terminal of the plurality of secondary windings. Each of the plurality of switches is substantially simultaneously switched by an input signal applied to the primary.

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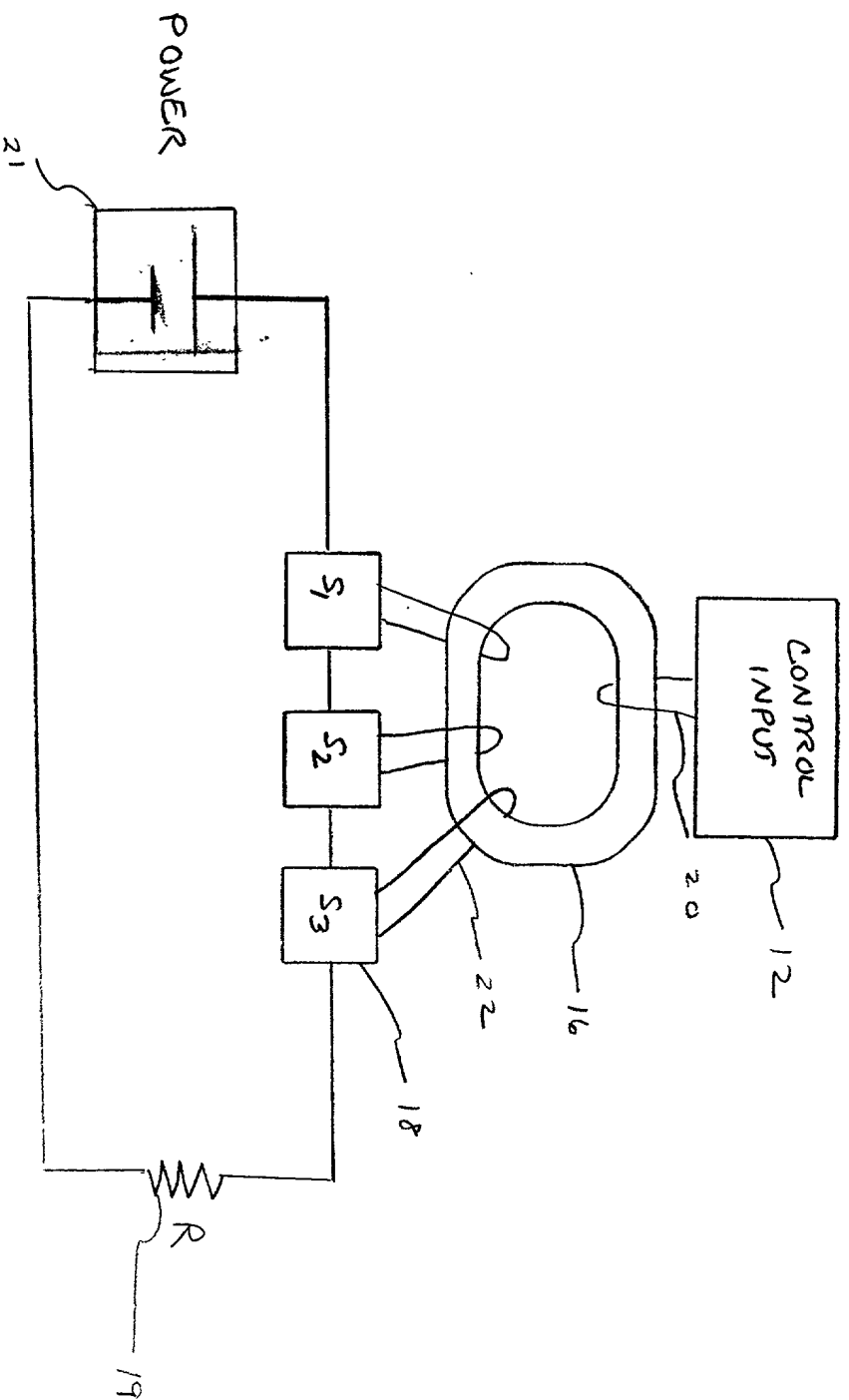


FIGURE 1

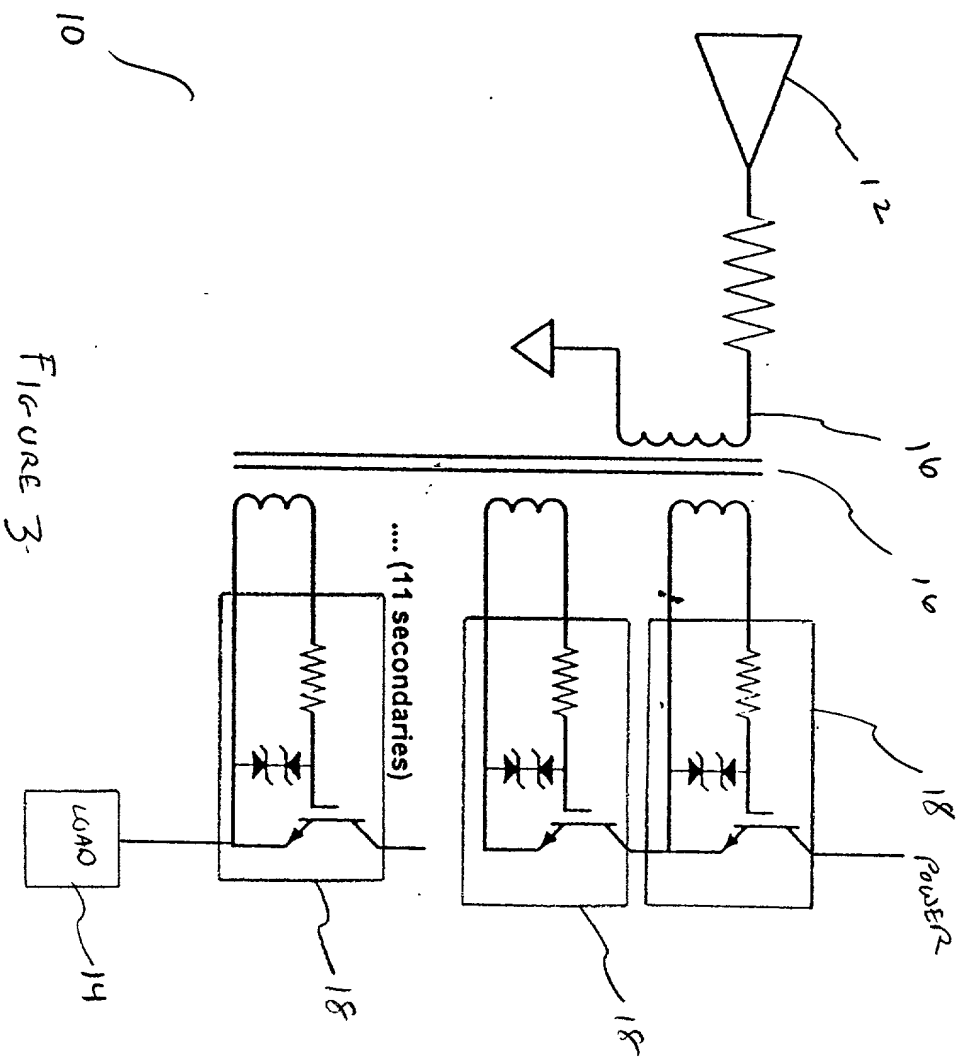


FIGURE 3-

A block diagram of a control system for a three-phase motor. A 'CONTROL' input line enters a square block labeled '12'. The output of block 12 is connected to a central oval-shaped component labeled '16'. A feedback line, labeled '20', connects the output of block 16 back to its input. The component 16 is connected to three square blocks labeled 'S1', 'S2', and 'S3', which are collectively labeled '18'. These blocks are connected to a three-phase power supply, represented by three vertical lines. A 'POWER' source, labeled '21', is connected to the bottom two lines of the three-phase supply. A 'LOAD' is connected to the top and bottom lines of the three-phase supply, with the label '14' pointing to the load block.

FIGURE 4

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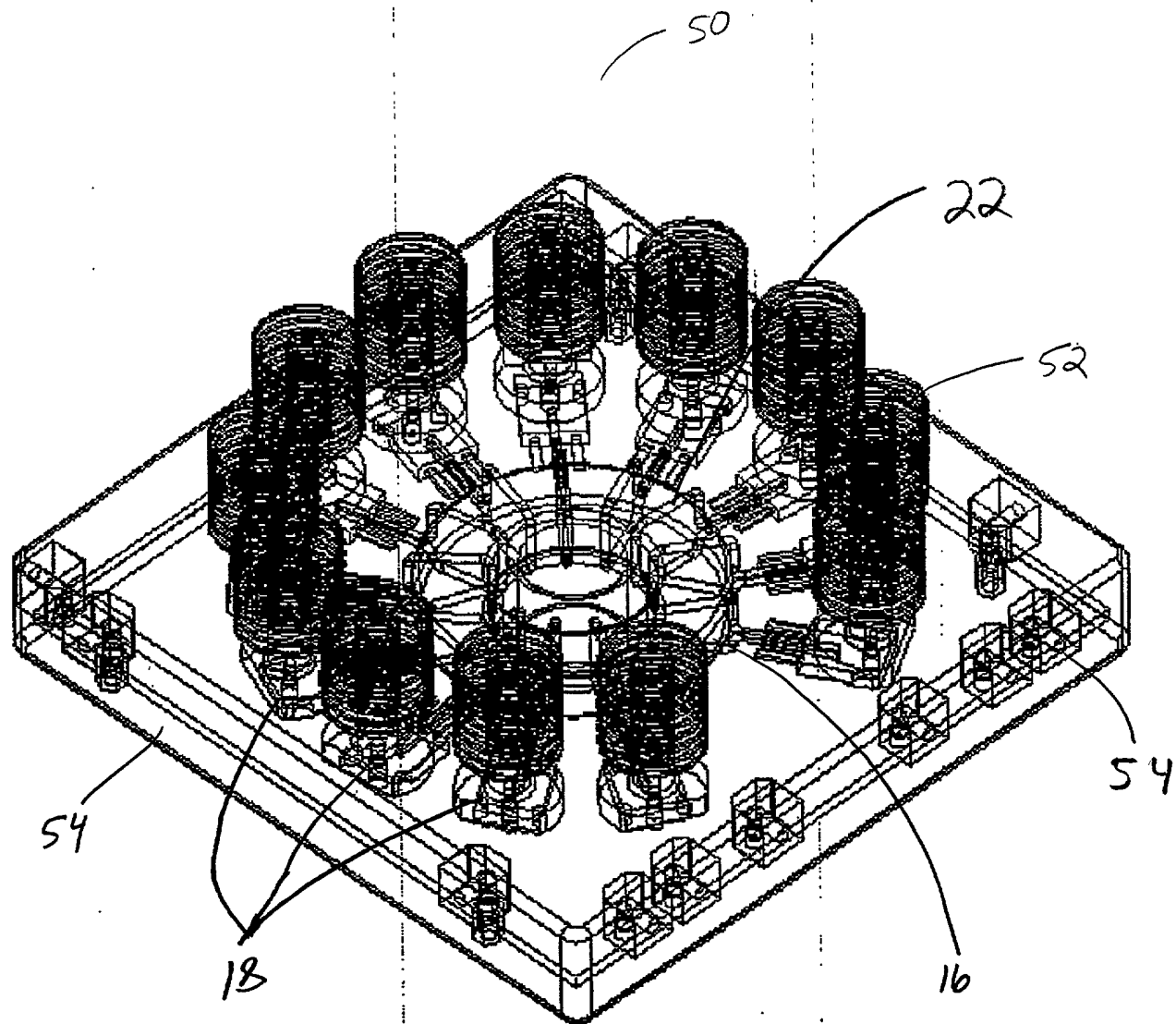
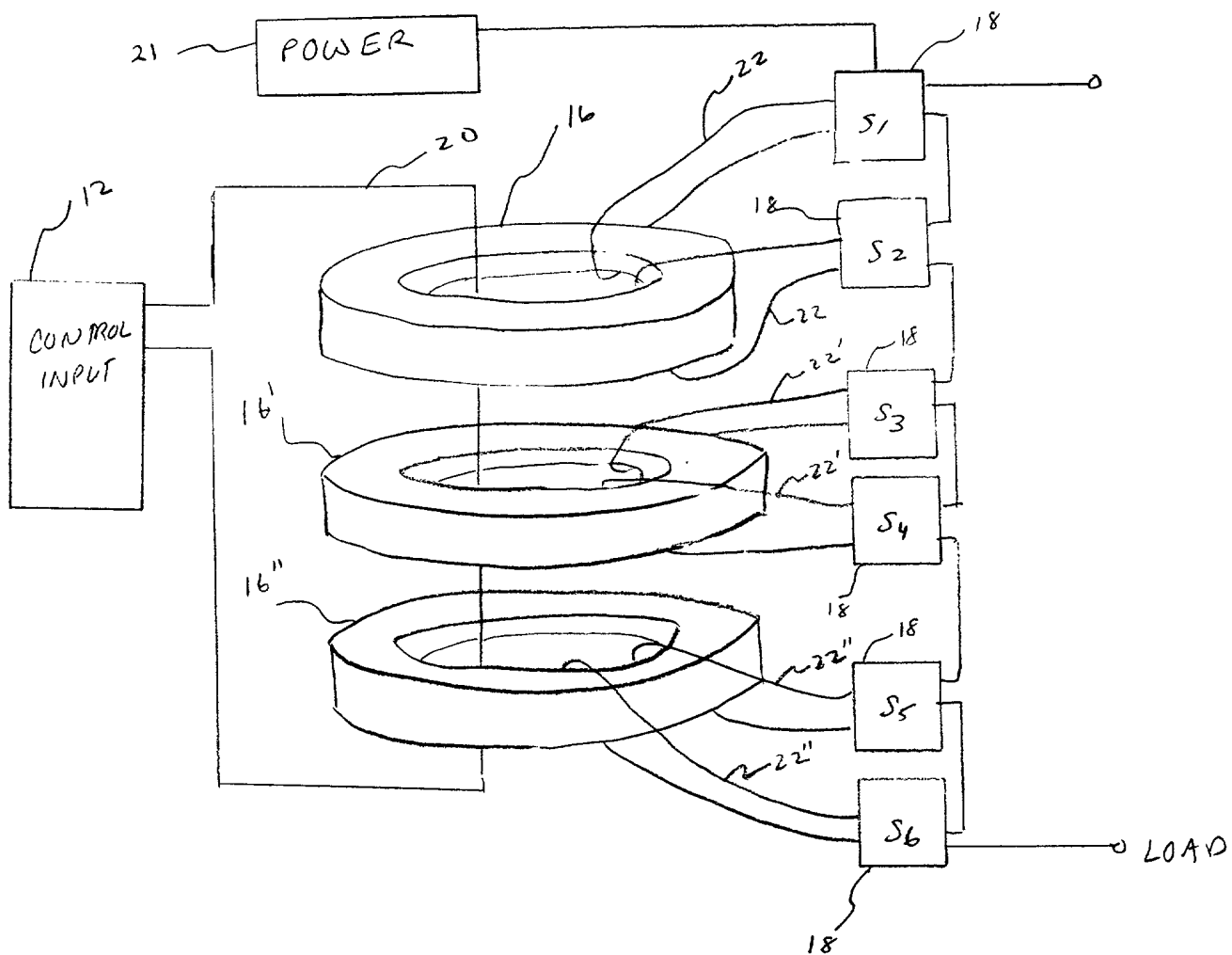


FIG. 5

	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431	2432	2433	2434	2435	2436	2437	2438	2439	2440	2441	2442	2
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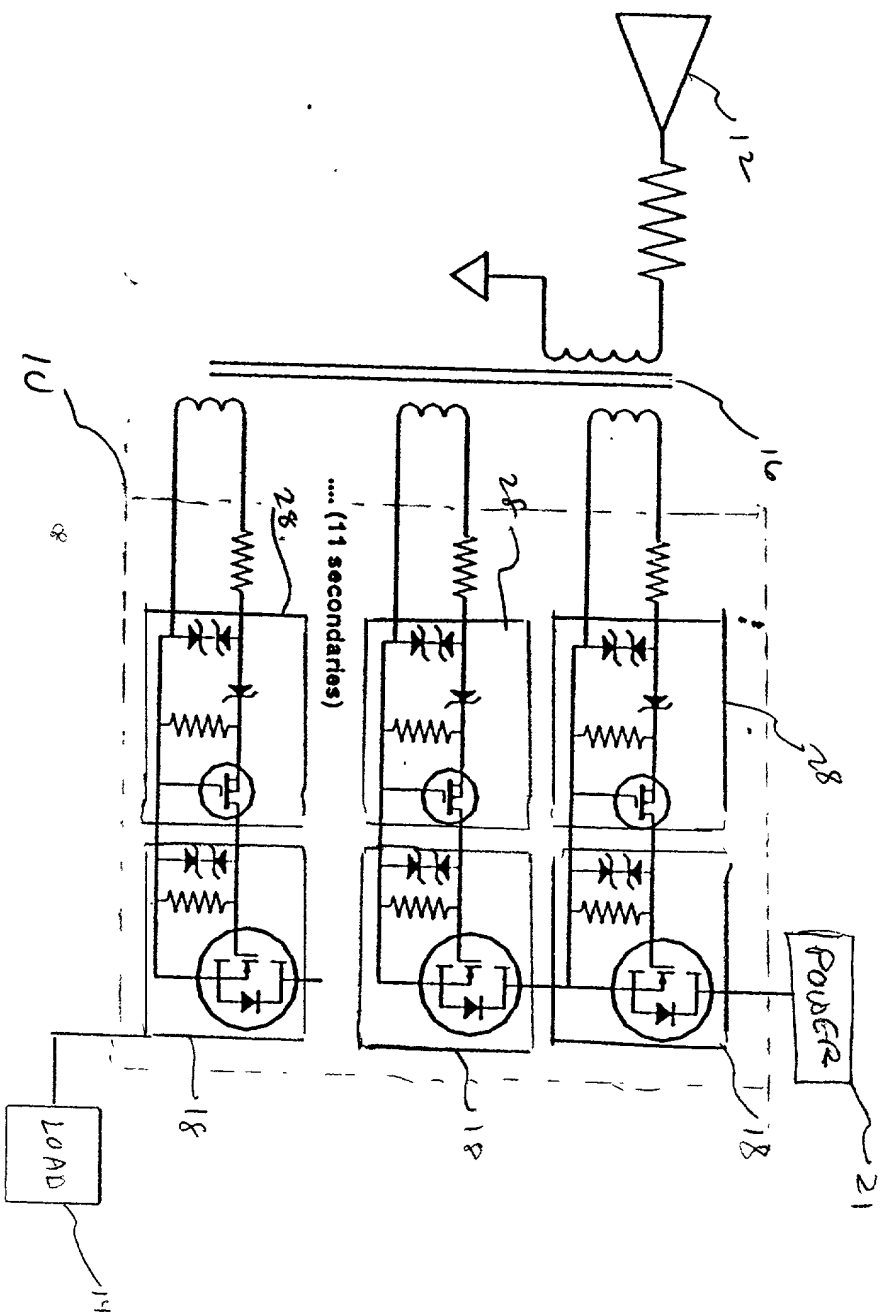


FIG. 7

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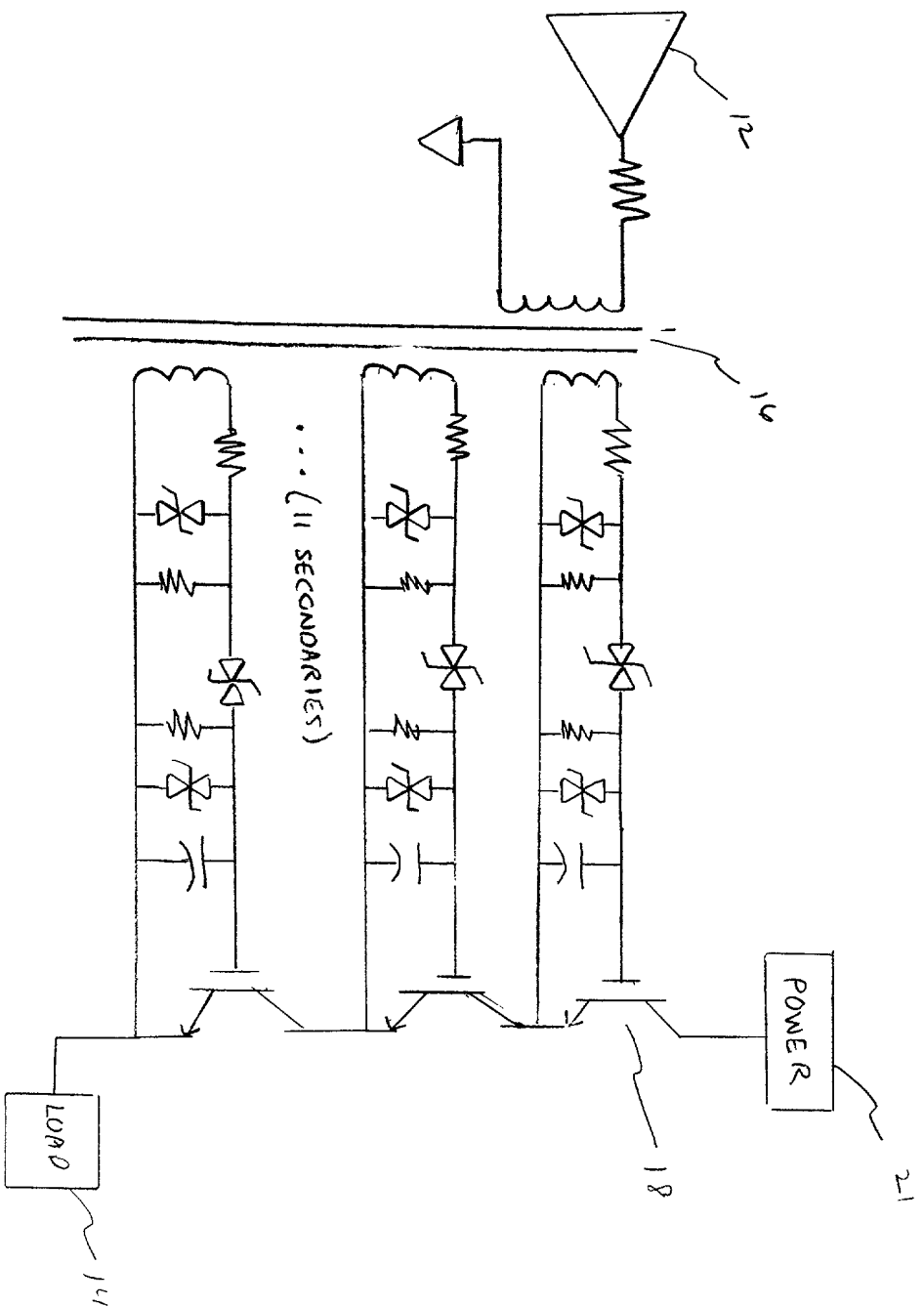


FIG. 8

DECLARATION AND POWER OF ATTORNEY FOR UTILITY OR DESIGN PATENT APPLICATION <input checked="" type="checkbox"/> Declaration <input type="checkbox"/> Declaration Submitted with Submitted after Initial Initial Filing Filing (surcharge 37 CFR 1.16(e) required)	Attorney Docket No.	DVS-007 (2516/8)
	First Named Inventor	Marcel P.J. Gaudreau
	COMPLETE IF KNOWN	
	Application Serial Number	Not Yet Assigned
	Filing Date	January 10, 2000
	Group Art Unit	Not Yet Assigned
	Examiner Name	Not Yet Assigned

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

High Power Modulator
(Title of the Invention)

the specification of which

☒ is attached hereto
OR
☐ was filed on as United States Application Serial Number or PCT International (MM/DD/YYYY)

Application Number and was amended on (MM/DD/YYYY) (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				YES	NO
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

☐ Additional foreign application numbers are listed on a supplemental priority data sheet attached hereto.

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Serial Number(s)	Filing Date (MM/DD/YYYY)

☐ Additional provisional application serial numbers are listed on a supplemental priority data sheet attached hereto.

DECLARATION - Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c), of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Serial Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet attached hereto.

As a named inventor, I hereby appoint the following registered practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: ☐ Customer Number

OR

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Parameter	Value	Unit
α	0.001	1/s
β	0.001	1/s
γ	0.001	1/s
δ	0.001	1/s
ϵ	0.001	1/s
ζ	0.001	1/s
η	0.001	1/s
θ	0.001	1/s
ι	0.001	1/s
κ	0.001	1/s
λ	0.001	1/s
μ	0.001	1/s
ν	0.001	1/s
ξ	0.001	1/s
\omicron	0.001	1/s
π	0.001	1/s
ρ	0.001	1/s
σ	0.001	1/s
τ	0.001	1/s
υ	0.001	1/s
ϕ	0.001	1/s
χ	0.001	1/s
ψ	0.001	1/s
ω	0.001	1/s
Ω	0.001	1/s
Θ	0.001	1/s
Φ	0.001	1/s
Ψ	0.001	1/s
Ξ	0.001	1/s
\Omicron	0.001	1/s
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\Omicron	0.001	1/s
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Ξ	0.001	1/s
\Omicron	0.001	1/s
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Υ	0.001	1/s
Φ	0.001	1/s
Ψ	0.001	1/s
Ξ	0.001	1/s
\Omicron	0.001	1/s
Π	0.001	1/s
Σ	0.001	1/s
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Φ	0.001	1/s
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Ξ	0.001	1/s
\Omicron	0.001	1/s
Π	0.001	1/s
Σ	0.001	1/s
Υ	0.001	1/s
Φ	0.001	1/s
Ψ	0.001	1/s
Ξ	0.001	1/s
\Omicron	0.001	1/s
Π	0.001	1/s
Σ	0.001	1/s
Υ	0.001	1/s
Φ	0.001	1/s
Ψ	0.001	1/s
Ξ	0.001	1/s
\Omicron	0.001	1/s
Π	0.001	1/s
Σ	0	

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Post Office Address																	
		City				State				Zip				Country			
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Inventor's Signature							Date										
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		City				State				Zip				Country			

DECLARATION AND POWER OF ATTORNEY FOR UTILITY OR DESIGN PATENT APPLICATION	ADDITIONAL INVENTOR(S) Supplemental Sheet Page 4 of 4
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Inventor's Signature						Date					
Street Address		30 Jericho Hill Road				Citizenship		U.S.A.			
		City	Southborough	State	MA	Zip	01772	Country	U.S.A.		
Post Office Address											
		City		State		Zip		Country			

Name of Additional Joint Inventor, if any:				<input type="checkbox"/> A petition has been filed for this unsigned inventor			
Given Name (first and middle [if any])				Family Name or Surname			
Peter A.				Dandrige			
Inventor's Signature						Date	
Street Address		13 Kensington Park				Citizenship	
		City		Lynn		State	
		MA		Zip		01902	
		Country		U.S.A.			
Post Office Address							
		City				State	
		Zip				Country	